

STANDARD PROCEDURES AND PRACTICES

Number: **SPP-020, Issue A**

Subject: **Rectangular Grid Array Terminal Position Numbering**

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Background

The numbering practice for grid array packages has been clearly defined for square packages in JEP95, Section 3, SPP-010. The application of this practice to rectangular array packages is ambiguous and has led to inconsistency in the numbering shown in JEDEC outlines.

Practice

All JEDEC registered or standard outlines for rectangular grid array packages shall use an alphanumeric system for designating pin or terminal locations. The required alphanumeric system is as defined in SPP-010. Array packages using this system shall have a uniquely identified corner that shall be known as the terminal A1 corner. The numbering system will be applied to rectangular packages so that alphabetic characters shall be associated with the major axis of the package body (dimension D), and numeric characters shall be associated with the minor axis of the package body (dimension E).

Application Information

A row-column grid system is used to designate the terminal positions on grid array packages having 3 or more rows or columns of terminals. The terminals may be solder balls, pins, metallized pads, or other forms. The numbering system will use a unique alphanumeric identification for each terminal position on such packages, e.g., A1, D12, or AB23, per JEP95, Section 3, SPP-010.

When a package is viewed in the as-mounted condition, the orientation of the grid system is as illustrated in Figure 1. When the package is viewed from the terminal or pin side, the orientation of the grid system is as illustrated Figure 2.

Recommended drawing practice is to show the top view with the A1 corner in the upper left corner and the package length defined by dimension D in the vertical direction as in Figure 1.

For DSBGA packages dimension D does not necessarily define the major package axis (see JEP95, Section 4.7), but the association of the alphabetic characters with dimension D shall be followed as illustrated in Figure 3.

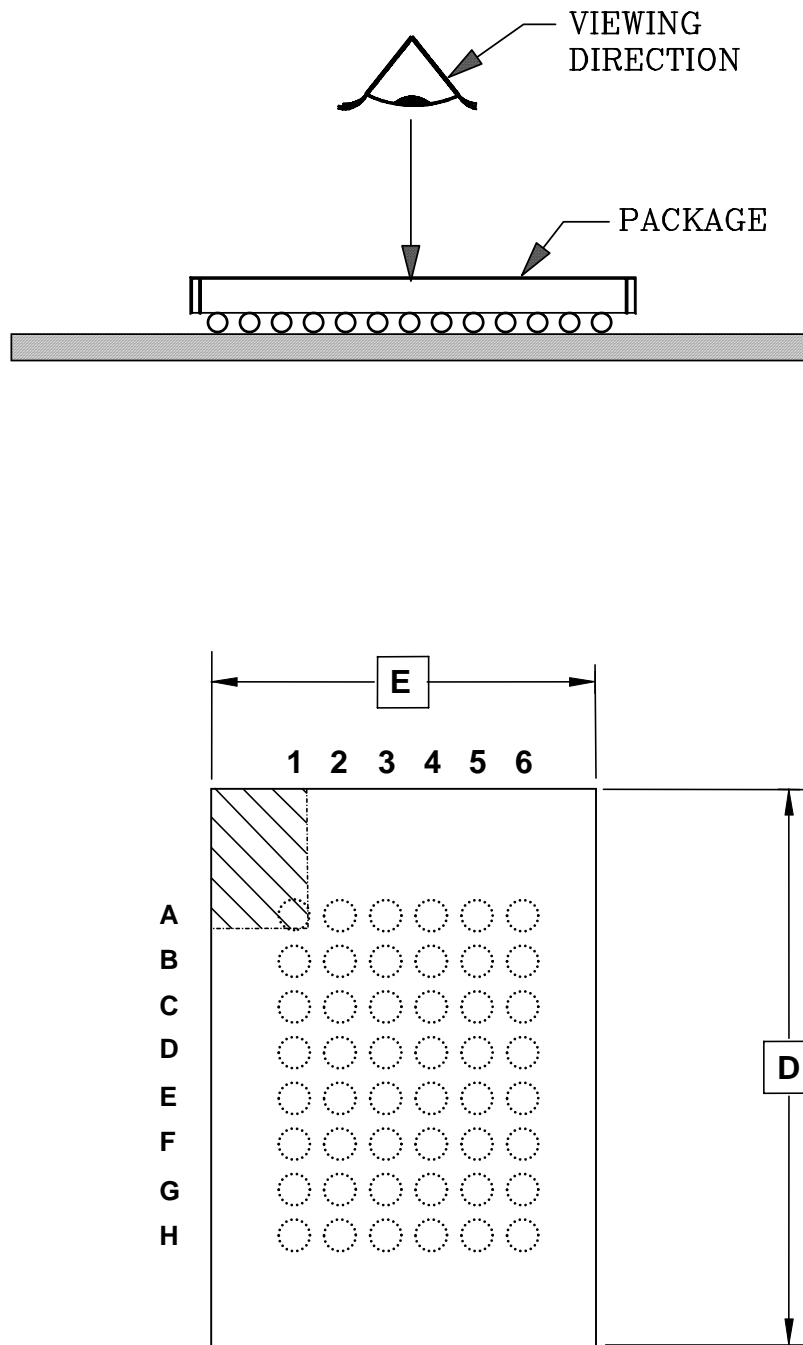


FIGURE 1

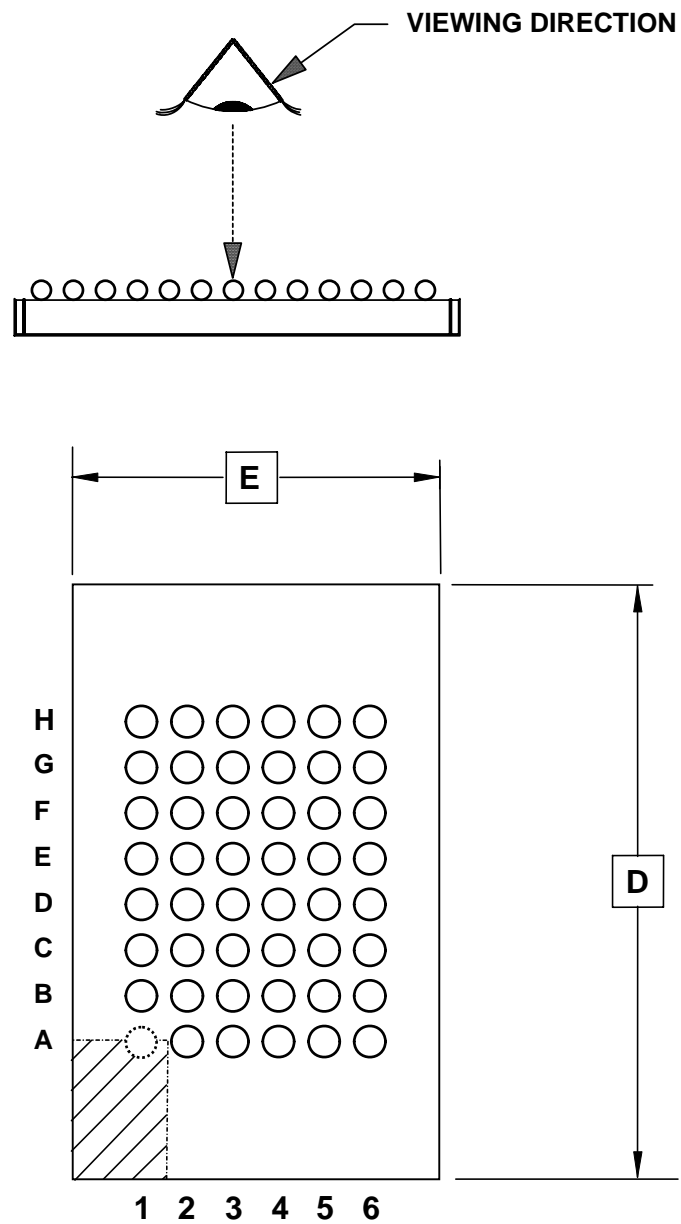


FIGURE 2

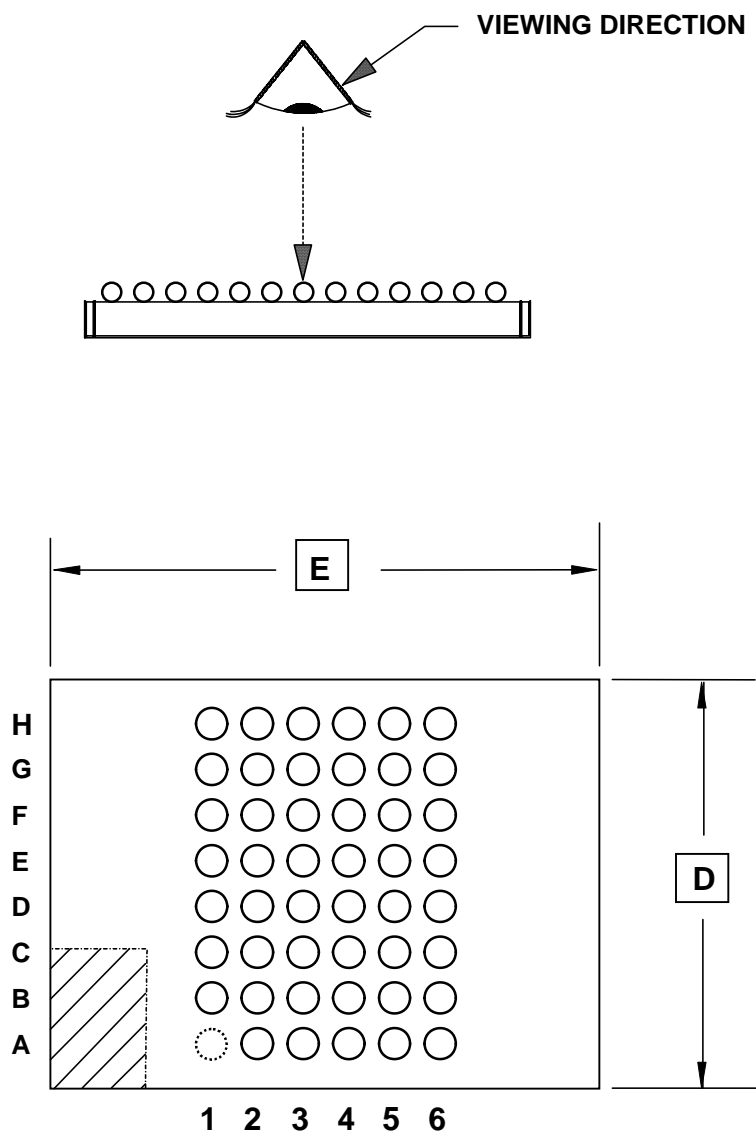


FIGURE 3
(DSBGA OPTION)